Amendments to the Specification

Pages 11-12, the paragraph bridging these pages, page 12, line 23 to page 12, line 11, replace the paragraph with:

A disk array control CPU 11008 is a processor for controlling a disk array. The disk array refers to a storage device consisting of a plurality of disks. Disk arrays in which at least one of a plurality of disks stores redundant data to provide fault tolerance are called RAIDs. RAIDs are described later. A disk array control memory 11009 is connected to the disk array control CPU 11008 and stores programs executed by the disk array control CPU ~~11009~~11008 and control data. An SM I/F control circuit 11005 is a circuit for controlling access from the CHNs 110x to the SM 13. A CM I/F control circuit 11006 is a circuit for controlling access from the CHNs 110x to the CM 14. An inter-CPU communication circuit 11007 is a communications circuit used when the file access control CPU 11001 communicates with the disk array control CPU 11008 in order to access disks.